EXCELLENCE BY DESIGN

BLT TECHNOLOGY SUMMIT 2024

Embedded & Programmable Solutions

Orlando, FL
10.22.24

Melbourne, FL
10.24.24

Columbia, MD
10.29.24

SPONSORED BY:

AMD

CUT DELAYS AND REDUCE ENGINEERING FRUSTRATIONS WITH PRACTICAL SOLUTIONS

Are you facing issues with ever-changing design environments, timing closure, architecture migration, or debugging? The BLT Technology Summit 2024 is tailored to tackle these head-on.

Join us for a full day of practical demos and insights into overcoming everyday challenges in embedded and programmable solutions with our expert-led sessions from BLT and AMD. Exclusively from BLT.

REGISTER:

DETAILS:
WHERE: In-person in Orlando, Melbourne and Columbia (see website for details)
TIME: 10 AM - 4 PM ET
COST: $100 per person (includes breakfast, lunch, and parking)

SEE BACK FOR AGENDA

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BLT TECHNOLOGY SUMMIT

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AGENDA

TIME	SESSION
9:00 - 10:00 am	**Registration & Breakfast**
10:00 - 10:10 am	**Opening Remarks**
10:10 - 11:00 am	**Go NoC or Go Home: The ONLY Way to Access Key Versal Resources** Do you know how to interface with the Versal NoC, configure dozens of pages in the NoC's configuration wizard(s), connect to DDR, or use ChipScoPy to accelerate debugging? The Versal NoC is the silver bullet for routing challenges. Learn how to solve your latency, bandwidth, routing and resource allocation issues, and when NOT to use the NoC. Includes a lecture and demo.
11:00 - 11:30 am	**Session Presented by AMD**
11:30 - 12:00 pm	**AXI Nightmares: Avoid and Debug Performance Bottlenecks** Frustrated tracing bugs in AXI's concurrent transactions? Does out-of-order data make debugging feel like finding a needle in a haystack? Get to the bottom of performance issues and arbitration delays in your AXI implementation and take the complexity out of AXI. Includes a lecture and a demo.
12:00 - 1:00 pm	**Lunch**
1:00 - 1:40 pm	**Migration Frustration: Navigating Steep Learning Curves with New FPGA Architectures and Tools** Is the fear of unknown risks and costs keeping you from migrating to newer devices? (Even if you have to?) Are you stressed about new and constantly evolving tools and technologies but need to migrate for higher performance, availability, bandwidth, and latency? Learn about common issues in migration, from IO clocking, transceivers, voltages, configurations, booting, and more. Also hear about common issues when migrating between like devices. Includes a lecture and a demo.
1:40 - 2:20 pm	**Back to Vivado Flow: Marty, This Is the Future** The Vitis Export to Vivado Flow turbocharges your SW/HW team collaboration and productivity. Are you a HW engineer with minimal visibility into SW development? Are you a SW engineer with limited visibility into HW development? This new feature for Vivado 2024.1 helps compress schedules and reduce team frustrations. Includes a lecture and demo.
2:20 - 2:30 pm	**Break**
2:30 - 3:10 pm	**Confronting FPGA Timing Failures and Cracking the Secrets of Complex Timing Reports** Are you still getting timing errors even after you've added all your timing constraints? Does it take overnight for the tools to try to meet timing? Learn the specifics of timing closure and how to read and leverage a timing report. Includes a lecture and demo.
3:10 - 3:50 pm	**5 Reasons FPGA Designs Fail: How to Prevent Them and Costly Delays** Are you finding bugs on the bench? Afraid you might not be catching them all? When simulation doesn't meet reality, it's usually one of 5 reasons. Learn what they are and how to prevent costly surprises and unpredictable outcomes. Includes a lecture and demo.
3:50 - 4:00 pm	**Closing Remarks**
4:00 - 4:30 pm	**Networking Opportunity**

REGISTER: www.bltinc.com/events/blt-technology-summit/