BLT Adaptive Computing Summit

Columbia, MD April 25 | **Melbourne, FL** May 2 | **Orlando, FL** May 4 | **Huntsville, AL** May 17

Agenda

TIME	TOPIC
8:00 - 9:00	Registration & Breakfast
9:00 - 9:15	Opening Remarks
9:15 - 10:00	RFSoC Case Study: SAR on Orbit • Low-Voltage IO for defense grade parts and considerations when using DDR4 • Reliable and Safe State Machines for LEO • Introduction to SAR and the benefits of a space-based approach
10:00-10:30	An Introduction to Versal, presented by AMD
10:30 - 10:45	Break
10:45 - 11:30	Common DSP function benchmarks (FIR, FFT and Matrix) – AIE vs. PL
11:30 - 12:00	Managing FPGA & SoC Projects: The Methodologies Behind BLT's Secrets to Success • BLT's design methodologies for successful projects on the first try, every time • How to make the tools work efficiently and quickly on large designs
12:00 - 1:00	Lunch
1:00 - 1:30	STAP Radar Design – Development Flow and Results
1:30 - 2:15	Versal Channelizer Benchmark (AI vs PL) • A comparison of results when implementing in Programmable Logic vs AI Engines • Expectations on power consumption • Trade-study between each approach
2:15 - 2:30	Break
2:30 - 3:00	DEMO: Cross Triggering Is Your (Powerful) Friend • Tips & tricks for debugging SoCs and systems which contain software and programmable logic • Live Demonstration which shows engineers how to enable this capability for their designs
3:00 - 3:30	System Mapping Tool – Deciding What Goes in AIE and What Goes in DSP58 (Versal)
3:30 - 4:00	Engineering Roundtable • Panel of Experts will provide valuable information and answer audience questions • Space, Security, or DFX (topic dependent on location) • Advanced Debugging Tips & Tricks for FPGA and SoC design
4:00	Closing Remarks
4:00 - 5:00	Networking Reception

https://bltinc.com/events/adaptive-computing-summit-southeast/